# AN INTEGRAL TOPSIDE VACUUM PACKAGE

## Background

The invention relates to sealed vacuum packages and particularly to wafer pairs sealed having sealed chambers. More particularly, the invention relates to such packages having wafer topcaps.

The present application is a Continuation-in-Part of U.S. patent Application No. 10/154,577, filed on May 23, 2002, by B. Cole, R.A. Higashi et al., and entitled "Multi-Substrate Package Assembly."

Several patent documents may be related to sealed wafer pair chambers integrated vacuum packages. One patent document is U.S. Patent No. 5,895,233, issued April 20, 1999, to R. Higashi et al., and entitled "Integrated Silicon Micropackage for Infrared Devices," which is hereby incorporated by reference in the present specification. The assignee of this patent is the same assignee of the present invention. Another patent document is U.S. Patent No. 6,036,872, issued March 14, 2000, to R.A. Wood et al., and entitled "Method for Making a Wafer-Pair Having Sealed Chambers," which is hereby incorporated by reference in the present specification. The assignee of this patent document is the same assignee of the present invention.

Still another patent document is U.S. Patent No. 6,627,892 B2, issued September 30, 2003, to B. Cole, and entitled "Infrared Detector Packaged with Improved Antireflection Element," which is hereby incorporated by reference in the present specification. The assignee of this patent document is the same assignee of the present invention.

## Summary

The present invention may have a substrate wafer with pixels and electronics, and a topcap wafer situated on and sealed to the substrate to form an integrated sealed package. The topcap may have an antireflective pattern formed on its interior surface proximate to the pixels. The topcap may have an inside volume around the perimeter of the pixels. Also, the topcap may have a sealable pumpout hole, vent or opening.

## Brief Description of the Drawings

Figures 1a and 1b show a cross-sectional view and bottom view of a topcap with an interior bump filter;

Figures 2a and 2b show a cross-sectional view and top view of the topcap with an exterior bump filter;

Figures 3a and 3b a show a cross-sectional view and bottom view top view of the topcap with a perimeter seal;

Figures 4a and 4b show cross-sectional view and bottom view of the topcap with interior recesses;

Figures 5a and 5b show a cross-sectional view and bottom view of the topcap with vent holes;

Figure 6 shows a cross-sectional view of the topcap wafer and the bottom wafer of the package prior to sealing of the wafers; and

Figures 7a and 7b show cross-sectional and top views of the assembled and sealed integrated vacuum package.

## Description

The present invention may be a wafer having CMOS electronics and a topcap sealed to the wafer resulting in an integral vacuum package. A group of pixels may be situated on the wafer. Related art integral vacuum packages may have pumpout holes in the CMOS wafers for providing vacuum to the packages. Such location of the pumpout holes may result in severe yield losses relative to the expensive CMOS wafers. Further, the shapes of the topcaps of those other packages do not permit making anti-reflective surfaces on the interior of

the topcaps to enhance pixel response. This is because the topcap has a shape with an interior surface what is a significant distance away from the pixels for a recess to permit for the dilution of components outgassed from the wafer package over time. The plane of the interior surface is also a significant distance from plane of the topcap seal. This configuration results in a shape of the interior surface that makes it impracticable if not impossible to provide the anti-reflective surface to the interior side of the topcap above the pixels. To avoid such impracticality, the present invention may change the recess from above the pixels to a perimeter volume around the group of pixels. Then the interior surface of the topcap may be near the pixels. This redesigned recess of the top may be used in conjunction with the pumpout holes or vents in the topcap wafer rather than the bottom pixel wafer. These changes may improve pixel performance and pixel or CMOS wafer yield.

Figure 1a shows a cross-section view of a topcap wafer 11. Wafer 11 is a float-zone wafer, i.e., having low oxygen content and being low-doped. The bottom or interior surface 29 of wafer 11 may have an antireflective surface 12. Surface 12 may be bumps 13 etched with a plasma etcher. A stepper may be needed

for printing the bump patterns. Bumps 13 may be smaller than the wavelength of light that is to pass through wafer 11. The height or depth 32 of the bumps, posts or pedestals 13 may be approximately $\lambda/4$. The cross-dimensions or width 33 of the bumps, posts or pedestals 13 may be from $\lambda/10$ to $\lambda/5$. The indexes of refraction of bumps 13 and the places of space between the bumps (e.g., air or vacuum) may be averaged. This average index may be appropriate for attaining maximum anti-reflective (AR) properties of surface 12. A plan view of AR surface 12 is shown in Fig. 1b.

Interior cavity surface 29 of package cover or wafer 11 also may have an antireflection element, indicated generally at area 12, extending at least over an area above the detector pixel 21 array, and preferably over a greater area of cavity surface 29. Element 12 may be a field of upstanding posts 13 extending from a ground 34 in the level of surface 29. As an illustrative example, posts 13 may be shown as right circular cylinders, and are arranged in a rectangular matrix of rows and columns in the field of element 12. The dimensions and spacing (periodicity) of posts 13 may depends upon the refraction index of the window material and the wavelength band of the incident radiation desired to be detected. To approximate a quarter-

wavelength antireflective layer 12, the height or depth 32 of posts 13 may be about $h=\lambda/(4n)$, where $\lambda$ is the approximate center of the wavelength band of interest, and n is the effective index of refraction of the field of element 12. Post height 32 may be typically in the range of 0.2 micron to 4 microns, corresponding to band centers from 3 to 60 microns. To avoid reflection at surface 29, it may be desirable to make $n=(n_w)^{1/2}$, where $n_w$ is the index of the solid window or wafer 11 material. Because posts 13 may be arranged in a pattern having symmetry in two orthogonal directions, n could be regarded as isotropic. The antireflective properties of the field of element 12 may be then the same for all polarizations of the incident radiation. The pattern could also have other shapes; for example, hexagonal posts 13 may permit higher packing density within the field of element 12.

In this illustrative example, the tops of posts 13 may be flush with interior surface 29 of the cavity, and their bottoms, the ground level 34, may lie beyond that surface into wafer 11. Alternatively, posts may be fabricated as holes extending below interior surface 29, having substantially the same cross-sectional area as posts 13. The term "posts" may be used here to denote both upstanding posts and depressed holes. The shapes

of the posts (or holes) may be round, square, rectangular, or have any other convenient cross section. It may be also possible to fabricate posts (or holes) having a non-vertical sidewalls; that is, the posts can be shaped to provide a varying cross section along their height, such as substantially pyramidal or conical, including frustum and other variations of these shapes where the cross section decreases along the height of the posts (or, equivalently, depth of holes). Such posts offer enhanced antireflection performance over a wider range of wavelengths.

A desired effective index n of the field of element 12 may depend upon $n_w$ and upon the fill factor or relative area $A = A_p/A_f$ of the posts $A_p$ to the total field $A_f$. An approximate relationship for the effective index may be:

$$n = \{[(1-A+An_w^2)(A+(1-A)n_w^2)+n_w^2]/[2(A+(1-A)n_w^2)]\}^{1/2}$$

For round pillars of diameter d and center-to-center spacing s, $A = (\pi/4)(d/s)^2$. The relative areas of other shapes may be calculated. For silicon, the fill factor may range from about 20 percent to about 60 percent, being about 40 percent in this example. Post spacing or periodicity should be less than any wavelength in the desired band to avoid diffraction and scatter; for a rectangular array, this may be also the spacing

between adjacent rows and columns. The lowest spacing may be determined by process limitations rather than by optical considerations. For a silicon cover 11 and a detector pixels 21 operating in the wave band of about 6-12 microns, square posts of side 1.5 microns may be spaced 2.3 microns apart.

An exterior anti-reflective bump pattern 14 may be etched on an opposite side 31 of wafer 11, as shown in Figures 2a and 2b. Bumps, posts or pedestals 13 of element 14 may have the same dimensions as those of element 12. Without elements 12 and 14, the transmitivity of wafer 11 may be only about 50 percent. With one of elements 12 and 14, the transmitivity of wafer 11 may be about 70 percent. With both elements 12 and 14, then the transmitivity of wafer 11 may be 90 percent or greater.

In Figures 3a and 3b, there may be a spacer layer 15 and a malleable layer 17 that are patterned to match a seal ring 18 of a thin layer of gold on a detector wafer 19, as in Figure 6. Ring 18 may be another material with the malleability and bonding qualities similar to gold. Layer 17 is for compensating for flatness differences between the two wafers being sealed to each other. About five microns of nickel may be used as spacer layer 15 to keep anti-reflective surface 12 and the remaining portion of lower surface 29 of wafer 11 within the perimeter of

seal ring 18 from touching pixels 21 of detector wafer 19. Other material may be used for the spacer layer 15. There may be a bonding material 16 between metal 15 and wafer 11. Solder may be used for layer 17. It may be several microns thick so as to allow the seals of the wafers 11 and 19 to match up since both wafers might not have the same flatness relative to each other. Other materials in lieu of solder may be used for layer 17 of the seal.

To provide volume within and between wafers 11 an 19, portions 22 may be etched away from wafer 11, as shown in Figures 4a and 4b. Wafer 11 may be about 500 microns thick at dimension 23. Portions 22 may be about 400 microns deep at dimension 24 leaving about 100 microns of wafer 11 at the top of portion or volume 22. Establishing volume 22 may involve one or more hour etch using a Bosch approach.

Volume 22 does not have to encircle the entire wafer 11. Figure 4b shows a plan view of the bottom surface 29 of wafer 11 where volumes 22 are revealed. Portions or volumes 22 may be interrupted at the corners of wafer 11 with structural support portions 25. At those portions 25, portion or volume 22 is not etched and the thickness of wafer 11 may remain at about 500 microns. Thus, wafer 11 may provide volume 22 and yet maintain

structural rigidity with portions 25. The deep recess, volume, trenches, or portions 22 may be etched by DRIE into the bottom side 29 of topcap wafer 11 to increase vacuum volume thereby making the device more tolerant of outgassing within the resulting sealed structure 27 occurring during its lifetime. Mechanical supports 25 may be present so that the middle region in the area of surface 12 does not appreciably deflect.

Small vent holes 26, which may regarded as pumpout ports, as shown in Figures 5a and 5b, may be etched from the top or exterior surface 31 of wafer 11. These ports, apertures, or holes 26 may provide for the final outgassing and sealing of structure 27 after wafers 11 and 19 are bonded to each other.

Topcap wafer 11 may be bonded to detector wafer 19 with heat at about 300 degrees C for a period of time necessary to achieve a satisfactory bond, generally less than an hour. Then, bonded wafer pair 27 may be baked out to remove outgas from pair or structure 27. The temperature during bake-out may be around 250 degrees C for about eight hours at a pressure of $10^{-6}$ Torr in a sealed vacuum environmental chamber. Holes 26 may be open during the bake-out. Then structure 27 may be left to cool down to room temperature for about 12 hours. In the meanwhile, the vacuum or pressure of the environment of structure 27 in the

chamber may remain at about $10^{-6}$ Torr or less, such as $10^{-7}$ Torr. Then, while under this pressure after cool-down, small vacuum apertures, ports, holes 26 may be sealed or plugged with a deposited layer 28. The material of layer 28 may be indium or 50 percent ratio mix of indium and lead. The bonded and sealed integral topside vacuum package 27 is shown in cross-sectional and top views in Figures 7a and 7b, respectively.

Although the invention has been described with respect to at least one illustrative embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present specification. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.